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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: JAMIN LING ET AL.

SERIAL NO.: 09/766,798 — Art Unit 2816

FILED: 01/22/2001

FOR: "ELECTROLESS Ni/Pd/Au METALLIZATION STRUCTURE FOR COPPER INTERCONNECT SUBSTRATE AND METHOD THEREFOR"

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231 on: June 18, 2001

Marvin A. Glazer
Name of Registered Rep.

Signature — June 18, 2001 Date

TRANSMITTAL LETTER

Honorable Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In regard to the above-identified patent application, Applicants hereby enclose the following:

1. Disclosure Statement;
2. Information Disclosure Citation Form PTO-1449; and
3. Copies of the cited references

Please charge any fees required by this paper to Deposit Account No. 03-0088. Two duplicate copies of this Transmittal Letter are also enclosed.

Respectfully submitted,

CAHILL, SUTTON & THOMAS P.L.C.

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DISCLOSURE STATEMENT

Honorable Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Please make of record in the above-identified patent application the references identified below. The references identified below should be considered during the examination of the present application.

In accordance with 37 C.F.R. §1.98, copies of the references listed below accompany this Disclosure Statement. Pursuant to MPEP §609, this Disclosure Statement is accompanied by Form PTO-1449, entitled "Information Disclosure Citation" listing the references set forth below.

A concise explanation of the relevance of each reference follows the listing thereof.

U.S. Patent No.	Inventor Name	Issue Date
4,808,769	Nakano et al.	02/28/89
4,857,671	Nakano et al.	08/15/89
4,970,571	Yamakawa et al.	11/13/90
5,212,138	Krulik et al.	05/18/93
5,291,374	Hirata et al.	03/01/94
5,380,560	Kaja et al.	01/10/95
5,747,881	Hosomi et al.	05/05/98

5,821,627	Mori et al.	10/13/98
5,906,312	Zakel et al.	05/25/99
6,040,239	Akram et al.	03/21/00
6,049,130	Hosomi et al.	04/11/00
6,077,723	Farnworth et al.	06/20/00
6,091,252	Akram et al.	07/18/00
6,094,058	Hembree et al.	07/25/00
6,097,087	Farnworth et al.	08/01/00

Abstract of Japanese Patent No. JP411140658A to Hitachi (Hasegawa, et al.), entitled "Substrate For Mounting Semiconductor And Its Production."

OTHER DOCUMENTS

Strandjord, A., et al., Break Through Developments in Electroless Nickel/Gold Plating on Copper Based Semiconductors, Int. Symp. Adv. Pkg. Mat. 2000, pp. 107.

Jang, J.W., et al., Crystallization of Electroless Ni-P Under Bump Metallization Induced by Solder Reaction, Int. Symp. Adv. Pkg. Mat. 1999, pp. 252.

Stepniak, F., Solder Flips Chip Employing Electroless Nickel: An Evaluation of Reliability and Cost, Inter. PACK 1997.

Ostmann, A., et al., Electroless Metal Deposition for Back-End Wafer Processes, Advancing Microelectronics, p. 23.

Ulrich, R., et al., Thermosonic Gold Wirebonding to Electrolessly-Metallized Copper Bondpads over Benzocyclobutene, Int. Conf. High Density Pkg. and MCMs 1999, pp. 260.

O'Sullivan, E., et al., Electrolessly deposited diffusion barriers for microelectronics, IBM J.R.&D., *Vol. 42, No. 5 - Electrochemical microfabrication.*

HBS Technical Proposal #990505-2.0SH, "HBS Mark II Automatic Electroless Nickel/Immersion Gold Plate Tool", dated May 1999.

Concise Explanation of the Relevance of the Above-Mentioned References

U.S. Patent No. 4,808,769 (Nakano et al.)

The Nakano '769 patent discloses (within its discussion of the background art) a wafer level process of depositing metal layers on aluminum contacts of a semiconductor wafer topped

off with gold bumps for joinder to film carriers. The described process includes the steps of laminating titanium over the aluminum contacts, laminating nickel over the titanium layer, laminating palladium over the nickel layer, and forming gold bumps over the palladium layer. This structure is described in the background portion of the patent specification (column 1).

U.S. Patent No. 4,857,671 (Nakano et al.)

The Nakano'671 patent discloses (within its discussion of the background art) a wafer level process of depositing metal layers on aluminum contacts of a semiconductor wafer topped off with gold bumps for joinder to film carriers. The described process includes the steps of laminating titanium over the aluminum contacts, laminating nickel over the titanium layer, laminating palladium over the nickel layer, and forming gold bumps over the palladium layer. This structure is described in the background portion of the patent specification (column 1).

U.S. Patent No. 4,970,571 (Yamakawa, et al.)

The '571 patent to Yamakawa, et al. discloses the dipping a semiconductor wafer having an aluminum electrode in a palladium solution, followed by electroless nickel deposition over the palladium-coated electrode.

U.S. Patent No. 5,212,138 (Krulik et al.)

The '138 Krulik, et al. patent discloses the use of palladium to act as a catalyst for electroless nickel plating over a copper substrate.

U.S. Patent No. 5,291,374 (Hirata et al.)

The Hirata '374 patent discloses a semiconductor wafer-level process wherein aluminum electrode pads are covered by a barrier metal, and then gold bumps are formed over the barrier metal. The barrier metal is a stack consisting of titanium, nickel, and then palladium; the gold bump is formed over the palladium layer.

U.S. Patent No. 5,380,560 (Kaja, et al.)

The '560 Kaja patent discusses the use of palladium salts as a seed material during electroless nickel plating over copper metal structures.

U.S. Patent No. 5,747,881 (Hosomi et al.)

The Hosomi '881 patent discloses essentially the same structure as the Hirata '374 patent.

U.S. Patent No. 5,821,627 (Mori et al.)

The Mori '627 patent discloses a similar structure to that described in the aforementioned Nakano patents. However, the Mori patent states that the wiring layer can be made of copper or aluminum. The Mori patent further states that the gold bumps can be formed over the palladium layer by electroplating.

U.S. Patent No. 5,906,312 (Zakel et al.)

The patent to Zakel '312 shows a wafer-level solder bump structure for flip chips. The solder bump includes a gold core "coated" with a diffusion barrier layer that includes nickel and palladium. The diffusion barrier is above and around the bump, rather than underneath it.

U.S. Patent No. 6,040,239 (Akram et al.)

The Akram '239 patent discloses the formation of metal stack layers by electroless plating, but this patent appears to be directed to methods of making temporary, rather than permanent, contact with electrode pads on semiconductor wafers.

U.S. Patent No. 6,049,130 (Hosomi et al.)

The Hosomi'130 patent discloses essentially the same structure as the Hirata '374 patent.

U.S. Patent No. 6,077,723 (Farnworth et al.)

The Farnworth '723 patent also discloses the formation of metal stack layers by electroless plating, but this patent appears to be directed to methods of making temporary, rather than permanent, contact with electrode pads on semiconductor wafers.

U.S. Patent No. 6,091,252 (Akram et al.)

The Akram '252 patent also discloses the formation of metal stack layers by electroless plating, but this patent appears to be directed to methods of making temporary, rather than permanent, contact with electrode pads on semiconductor wafers.

U.S. Patent No. 6,094,058 (Hembree et al.)

The Hembree '058 patent also discloses the formation of metal stack layers by electroless plating, but this patent appears to be directed to methods of making temporary, rather than permanent, contact with electrode pads on semiconductor wafers.

U.S. Patent No. 6,097,087 (Farnworth et al.)

The Farnworth '087 patent discloses a chip-scale semiconductor package formed by a wafer-level process using copper metallization, a nickel/palladium land pad (41) deposited by electroless deposition, and metal solder bumps (40) formed over the land pads; the solder balls can be formed by electroless deposition. In one such embodiment, the solder bumps are formed of gold.

Abstract of Japanese Patent No. JP411140658A to Hitachi

The Abstract of Japanese Patent No. JP411140658A to Hitachi (Hasegawa, et al.), entitled "Substrate For Mounting Semiconductor And Its Production," states that an electroless nickel plating film is formed over a copper metal circuit, that an electroless palladium plating film is formed over the nickel film, and that an electroless gold plating film is formed over the palladium film.

Strandjord, A., et al., Break Through Developments in Electroless Nickel/Gold Plating on Copper Based Semiconductors

The technical article by Strandjord, et al. relates to the fabrication of integrated circuits using copper conductors, and regarding interfacing to copper input/output pads on such integrated circuits. It mentions the use of electroless nickel coupled with immersion gold on copper pads.

Jang, J.W., et al., Crystallization of Electroless Ni-P Under Bump Metallization Induced by Solder Reaction

The technical article by Jang, et al. discusses the use of an under-bump-metal (UBM) layer formed from electroless Ni-P plated over aluminum. A gold layer is formed over the electroless Ni-P layer, and a eutectic Sn-Pb solder bump is formed thereover.

Stepniak, F., Solder Flip Chip Employing Electroless Nickel: An Evaluation of Reliability and Cost

The technical article by Stepniak describes the use of a solderable electroless nickel film plated over aluminum. The electroless nickel is described as an interposer layer between the IC aluminum bond pad and the solder. A gold layer is deposited over a nickel bump.

Ostmann, A., et al., Electroless Metal Deposition for Back-End Wafer Processes

The technical article by Ostman, et al. describes the use of electroless nickel bumping on aluminum bond pads, but it mentions that Ni bumping on wafers with copper metallization is under current investigation. It also described the plating of a gold layer over the nickel layer.

Ulrich, R., et al., Thermosonic Gold Wirebonding to Electrolessly-Metallized Copper Bondpads over Benzocyclobutene

The technical article by Ulrich, et al. mentions the application of a nickel layer over a copper pad, and a gold overlayer applied over the nickel layer. Ulrich, et al. mention that both the nickel layer and the gold layer can be applied by electroless plating.

O'Sullivan, E., et al., Electrolessly deposited diffusion barriers for microelectronics

This article from the IBM Journal of Research and Development describes an integrated circuit using copper interconnect layers, copper input/output pads, and electroless nickel

HBS Technical Proposal #990505-2.0SH, "HBS Mark II Automatic Electroless Nickel/Immersion Gold Plate Tool," dated May 1999

This proposal was provided to assignee Flip Chip Technologies, LLC in or about May of 1999 by HBS Equipment Corporation of Los Angeles, California. The equipment described therein can be used in practicing the invention described and claimed in the present application, but it is not believed that this proposal discloses or suggests such invention.

Respectfully submitted,

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